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(54) IMPROVEMENTS IN AND RELATING TO INSULATED GATE SEMICONDUCTOR DEVICE

(71) We, MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD., a corporation organized under the laws of Japan, of 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to an insulated gate semiconductor device and more particularly to insulated gate thyristors of low V_T and insulated gate thyristors of high breakdown voltage. More specifically, the invention is intended to improve on the punching-through of the prior-art insulated gate semiconductor devices.

In the MOS transistor which is one class of the insulated gate transistor, it is usually desirable to minimize V_T, i.e. the lowest gate voltage required for forming a channel. To this end, the resistivity of the semiconductor in which a channel is to be formed is desirably as high as possible. However, the intent to increase the resistivity is likely to cause spreading of the drain side depletion layer, tending to result in punching-through. To avoid this, the gate gap may be increased, which however results in inferior frequency characteristics.

According to the present invention there is provided an insulated gate semiconductor device comprising a semiconductor substrate, which is provided on one principal surface with separate regions of opposite conductivity type from that of said substrate and separate low resistivity regions of the same conductivity type as but of lower resistivity than that of said substrate, said low resistivity regions extending in zones of maximum field intensity between said separate regions, and a gate electrode provided via an insulating layer on said substrate between said separate regions.

The invention will now be described by way of example only with particular reference to the accompanying drawing, in which:

Fig. 1 is a top view of a prior-art MOS transistor;

Fig. 2 is a top view of an embodiment of the insulated gate semiconductor device of the present invention;

Figs. 3 and 4 are fragmentary top views showing other embodiments of the invention; and

Fig. 5 is a top view showing still another embodiment of the invention.

Fig. 1 is a top view of an example of the prior-art MOS transistor. It comprises an n-type semiconductor substrate 1 of high resistivity. Numerals 2 and 3 designate p-type regions, with the region 2 constituting a source region and region 3 constituting a drain region. Numeral 4 designates a source electrode in ohmic contact with the source region 2, numeral 5 a drain electrode in ohmic contact with the drain region 3, and numeral 6 a gate electrode formed on an insulating layer. The cut-off frequency of the transistor is increased by reducing the gate gap, i.e., the distance between the regions 2 and 3. However, when the gate gap is reduced, the depletion layer on the drain side is likely to extend into the source side, resulting in punching-through. Therefore, the gate cap cannot be made excessively small.

The invention is based on the finding that the above drawback can be overcome by providing low resistivity regions in maximum field intensity zones between the source and drain.

Fig. 2 shows one embodiment of the invention. Referring to the Figure, numeral 7 designates an n-type semiconductor substrate, numerals 8 and 9 p-type regions, with region 8 serving as source and region 9 serving as drain, numeral 10 a source elec-

trode in ohmic contact with the source region 8, numeral 11 a drain electrode in ohmic contact with the drain region 9, numeral 12 a gate electrode formed on an insulating layer, and numerals 13 n^+-type regions, which constitute the characterizing feature of the invention and which have a lower resistivity than that of the substrate 7. The n^+-type regions 13 are formed in maximum field intensity zones between the source and drain. With this structure, the gate gap may be reduced without resulting in the punching-through of the drain side depletion layer into the source side. Also, the resistivity of the semiconductor substrate may be increased. Thus, with this structure it is possible obtain a low V_T transistor for high frequency purposes.

In the preceding embodiment of Fig. 2, the n^+-type regions 13 overlap source 8 and drain 9. For the principal purpose of preventing the punching-through of the drain side depletion layer, however, the n^+-type region formed in the maximum field intensity zone between the source and drain regions 8 and 9 need not extend across the entire gate gap, but it may extend across only part of the gap, as shown in Fig. 3.

Fig. 4 shows another possible layout, in which the n^+-type region 13 is formed in part of the substrate 7 and extends across the entire gate gap.

Although Figures 3 and 4 show only a single n^+-type region 13, it is to be understood that in each of these embodiments, there are two such regions, as in Figure 2.

While in the preceding embodiments the conductivity types of the various parts are predetermined for the sole sake of facilitating the description, the same effects of the invention may of course be obtained by selecting the opposite conductivity type for only the individual parts.

Some detailed examples of the invention will now be given.

EXAMPLE 1

A MOS transistor of a structure as shown in Fig. 2 was fabricated by diffusing boron into an n-type silicon substrate to form the source and drain regions and forming the n^+-type regions in the illustrated positions by the diffusion of phosphorus. An SiO_2 layer is used as the insulating layer. With this transistor, V_T of 1 volt and the cut-off frequency of 500 MHz were obtained.

EXAMPLE 2

A semiconductor device of a structure as shown in Fig. 5 was fabricated. Boron was selectively diffused into a n-type semiconductor substrate 7 to form p-type regions 8 and 9. Then, phosphorus was selectively diffused to form an n^+-type region 9' within the p-type region 9 as well as forming n^+-type regions 13. Numerals 10 and 11 respectively designate anode and cathode electrodes, and numeral 12 designates a gate electrode. This semiconductor device is an insulated gate thyristor, in which current controlled negative resistance is provided between the anode 10 and cathode 11, and its switching voltage can be controlled with the gate voltage. By the provision of the n^+-type regions 13 the resistivity of the semiconductor substrate can be increased to increase the breakdown voltage. With the above planar structure a breakdown voltage of 1,000 volts was obtained.

The above semiconductor devices are also sensitive to light, and they can provide high sensitivity and high switching speed as the light-sensitive semiconductor device.

While silicon is used as the semiconductor substrate in the above examples, other well-known semiconductors such as germanium, GaAs, GaP and InAs may also be used.

As has been described in the foregoing, the insulated gate semiconductor device according to the invention can be used as low-power high-frequency transistor and high breakdown voltage thyristor, so that it is very useful in industry.

WHAT WE CLAIM IS:—

1. An insulated gate semiconductor device comprising a semiconductor substrate, which is provided on one principal surface with separate regions of opposite conductivity type from that of said substrate and separate low resistivity regions of the same conductivity type as but of lower resistivity than that of said substrate, said low resistivity regions extending in zones of maximum field intensity between said separate regions, and a gate electrode provided via an insulating layer on said substrate between said separate regions.

2. A semiconductor device as claimed in claim 1 wherein the low resistivity regions extend only partially across the gap between said separate regions.

3. A semiconductor device as claimed in claim 2 wherein said separate regions constitute source and drain regions of an MOS transistor.

4. A method of fabricating the semiconductor device claimed in claim 1 and substantially as described in Example 1 referred to hereinbefore.

5. A method of fabricating the semiconductor device claimed in claim 1 and

substantially as described in Example 2 referred to hereinbefore.

6. A semiconductor device substantially as hereinbefore described and as shown in Figures 2 or 3 or 4 or 5 of the accompanying drawings.

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2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 1

FIG. 1 PRIOR ART

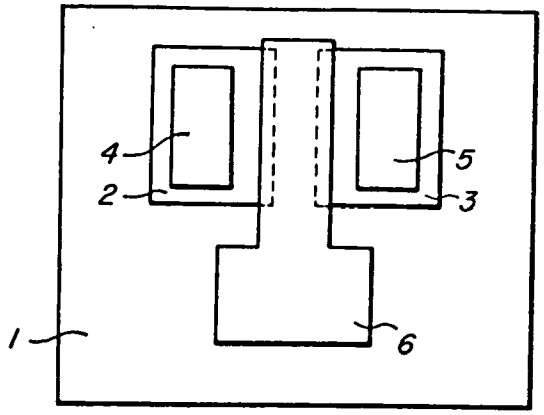

FIG. 2

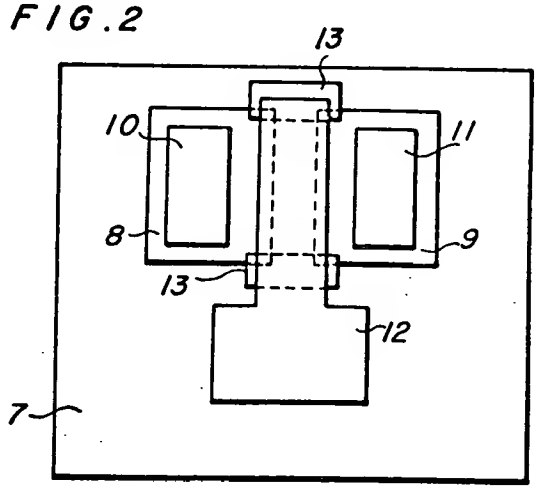

FIG. 3

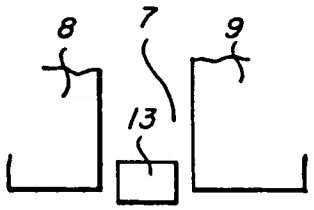

FIG. 4

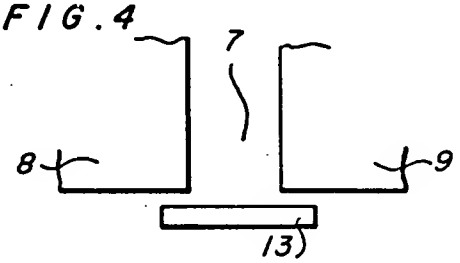

FIG. 5